# SGS-THOMSON MICROELECTRONICS

M62940A

VERY FAST CMOS 32K x 9 CACHE BRAM

- 32K x 9 CMOS SYNCHRONOUS BURST SRAM

- FAST CYCLE TIMES: 15, 20ns

- FAST ACCESS TIMES: 11, 12, 14ns Max

- ON-BOARD BURST COUNTER

- INPUT REGISTERS (ADDR.,DATA,CTRL)

- SELF-TIMED WRITE CYCLE

- THREE STATE COMMON I/O

- HIGH OUTPUT DRIVE CAPABILITY

- ASYNCHRONOUS OUTPUT ENABLE ($\overline{G}$)

- BURST CONTROL INPUTS: $\overline{TSP}$, $\overline{TSC}$, $\overline{BAA}$

- DUAL CHIP SELECTS for EASY DEPTH EXPANSION

PLCC44 (Q)
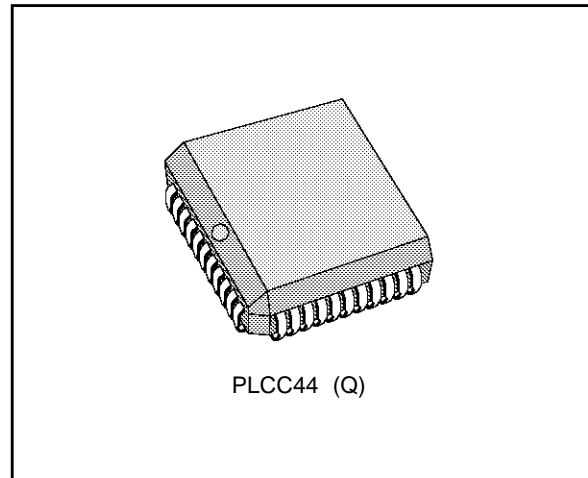
DESCRIPTION

The M62940A BRAM™ is a 288K (294,912 bit) CMOS Burst SRAM, organized as 32,768 words x 9 bits. It is fabricated using SGS-THOMSON's low power, high performance, CMOS technology.

Figure 1. Logic Diagram

Table 1. Signal Names

A0 - A14	Address Inputs
DQ0 - DQ8	Data Inputs / Outputs
K	Clock
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
S0	Chip Select 0, Active High
$\overline{S1}$	Chip Select 1, Active Low
$\overline{TSP}$	Address Start Processor
$\overline{TSC}$	Address Start Cache Controller
$\overline{BAA}$	Burst Address Advance
V_{CC}	Supply Voltage
GND	Ground
V_{CCQ}	Supply Voltage (DQ)
GND_Q	Ground (DQ)
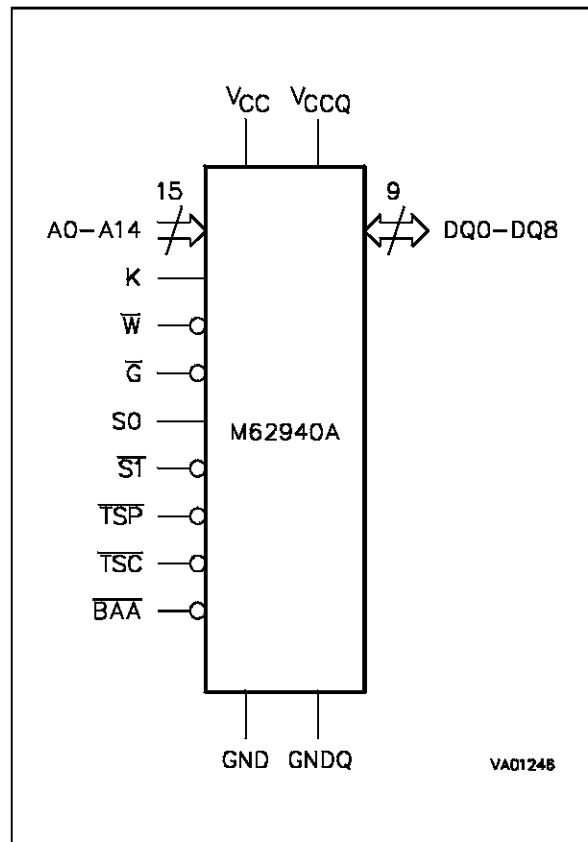
Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	−65 to 150	°C
V_{IO} [2]	Input or Output Voltages	−0.5 to 7	V
V_{CC}	Supply Voltage	−0.5 to 7	V
I_O [3]	Output Current	20	mA
P_D	Power Dissipation	1.2	W

Notes: 1. Except for the rating "Operating Temperature Range" stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Up to a maximum operating V_{CC} of 5.5V only.
3. One output at a time, not to exceed 1 second duration.

Figure 2. LCC Pin Connections
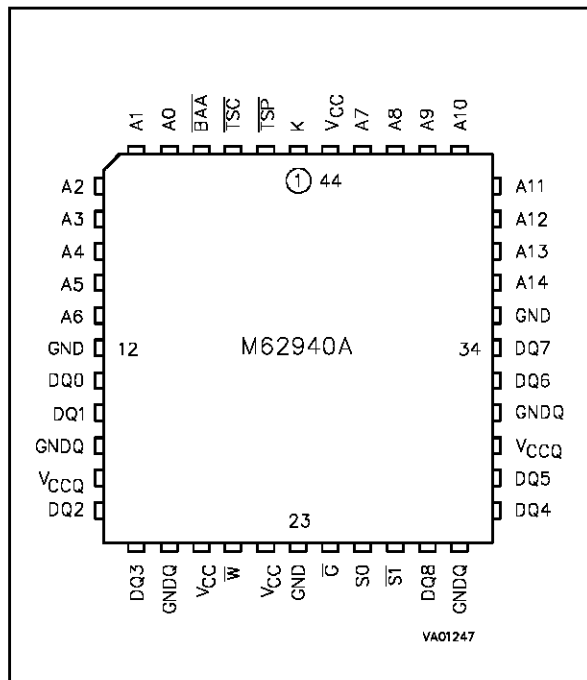
DESCRIPTION (cont'd)

The device integrates a 2-bit burst counter, input registers, high output drive capability, and high speed synchronous SRAM onto a single chip. The synchronous design provides precise control using an external clock (K) input. The M62940A is specifically adapted to provide a burstable, high performance secondary cache for the MC68040 microprocessor.

The device is pin compatible and functional equivalent to the Motorola MCM62940. The M62940A is available in a 44 lead Plastic Leaded Chip Carrier package (PLCC).

The device provides multiple power and ground pins to reduce effects induced by output noise for high performance applications. Separate power and ground pins (V_{CCQ} and GND_Q) have been employed for DQ0-DQ8 to allow output levels referenced to 5V or 3.3V. For proper operation all GND and GND_Q pin must be connected to ground. $V_{CC} \geq V_{CCQ}$ at all times including power-up. The main Burst SRAM power requires a single 5V ± 5% supply, and all inputs and outputs are TTL compatible.

DEVICE OPERATION

Addresses (A0-A14), data inputs (DQ0-DQ8), and control signals, with exception of Output Enable ($\overline{G}$) are clock controlled inputs through non-inverting, positive edge triggered registers. A cache burst address sequence can be initiated by either $\overline{TSP}$ (Transfer Start Processor) or $\overline{TSC}$ (Transfer Start Cache Controller) inputs, with subsequent burst addresses being internally generated by the Burst SRAM.

The $\overline{BAA}$ input (Burst Address Advance) provides control of the burst sequence, which imitates the required MC68040 cache burst address sequence. A cache burst cycle begins by loading the internal counter with the present values of A1 and A0. Thereafter, subsequent burst addresses are generated internally. The burst counter operates in the same manner for either cache burst write or read cycles.

Table 3. Asynchronous Truth Table

Mode	$\overline{G}$	DQ Status
Read	L	Data Out
Read	H	High-Z
Write[2]	X	Data In
Deselect	X	High-Z

Note: 1. X = Don't Care.
2. For a cache write cycle following a read operation, $\overline{G}$ must be high before the input data required set-up time, and be held high through the input data hold time.

Figure 3. Burst Count Sequence
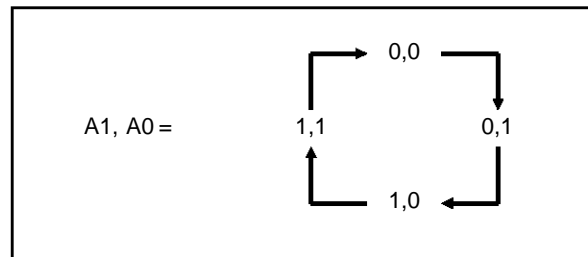
Note: The external values for A1, A0 are the starting point for the burst sequence graph. The burst counter will internally advance A1 and A0 as shown. After the counter reaches a full count from the initial value, the address will wrap around.

Table 4. Synchronous Truth Table

S0	$\overline{S1}$	$\overline{TSP}$	$\overline{TSC}$	$\overline{BAA}$	$\overline{W}$	K	Address	Operation
L	X	L	X	X	X	↑	N/A	Deselected
X	H	H	L	X	X	↑	N/A	Deselected
H	L	L	X	X	X	↑	External Base Address	Read Cycle - Begin Burst
H	L	H	L	X	L	↑	External Base Address	Write Cycle - Begin Burst
H	L	H	L	X	H	↑	External Base Address	Read Cycle - Begin Burst
X	X	H	H	L	L	↑	Advance Burst Address	Write Cycle - Continue Burst Sequence
X	X	H	H	L	H	↑	Advance Burst Address	Reade Cycle - Continue Burst Sequence
X	X	H	H	H	L	↑	Hold Current Burst Address	Write Cycle - Suspend Burst Sequence
X	X	H	H	H	H	↑	Hold Current Burst Address	Read Cycle - Suspend Burst Sequence

Notes: 1. X = Don't Care.

2. All inputs except $\overline{G}$ require set-up and hold times to the rising edge (low to high transition) of the external clock (K).

3. All read and write timings are referenced from $\overline{G}$ or K.

4. A read cycle is defined by $\overline{W}$ high or $\overline{TSP}$ low for the required set-up and hold times. A write cycle is defined by $\overline{W}$ being asserted low for the set-up and hold times.

5. $\overline{G}$ is a don't care when $\overline{W}$ is registered low from the previous rising clock edge.

6. Chip Selects must be true (S0 = high, S1 = low) at each rising of the clock while $\overline{TSP}$ or $\overline{TSC}$ is asserted for the device to remain enable; Chip Selects are registered whenever $\overline{TSP}$ or $\overline{TSC}$ is asserted low at the rising edge of the clock.

7. Chip Selects must be true (S0 = high, $\overline{S1}$ = low) at each rising of the clock while $\overline{TSP}$ or $\overline{TSC}$ is asserted for the the device to remain enabled; Chip Selects are registered whenever $\overline{TSP}$ or $\overline{TSC}$ is asserted low at the rising edge of the clock.

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Figure 4. Block Diagram
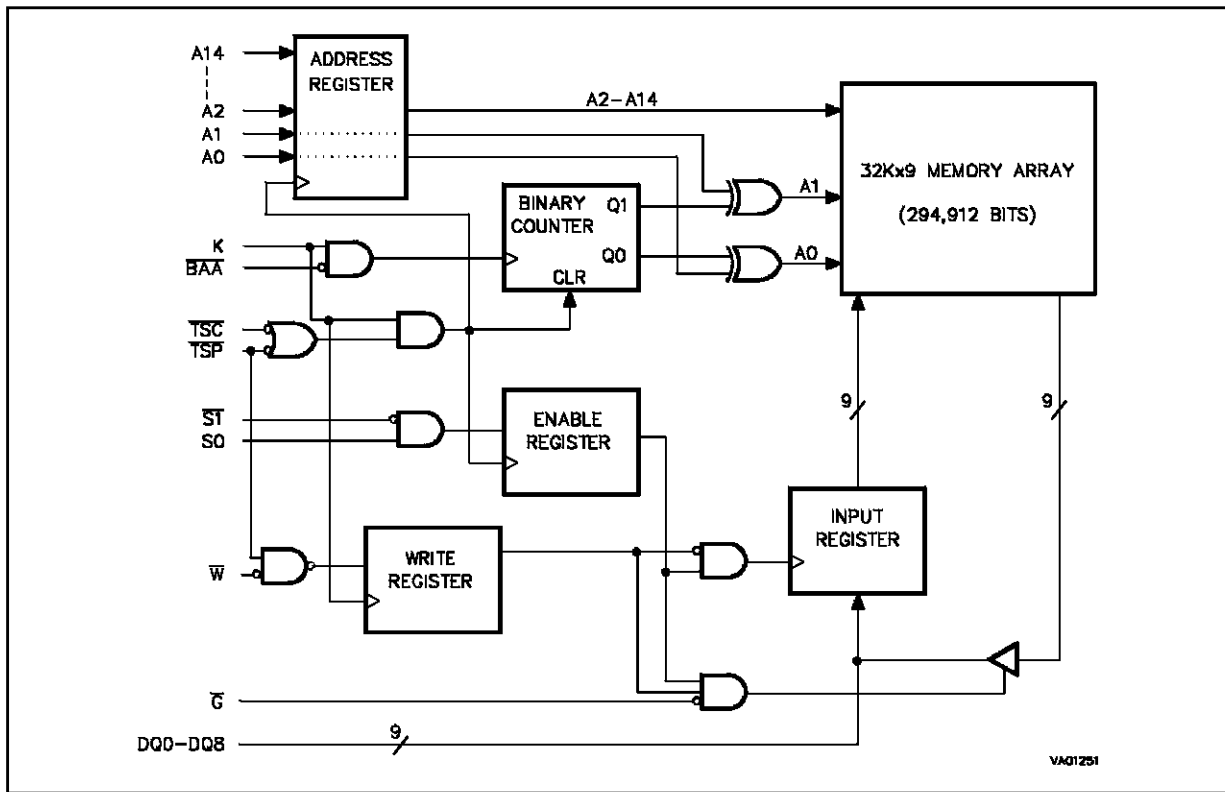
DEVICE OPERATIONS (cont'd)

The $\overline{\text{TSP}}$ and the $\overline{\text{TSC}}$ inputs control the start of the burst sequence. When either $\overline{\text{TSx}}$ is asserted low at the rising edge of the clock, any ongoing burst cycle is interrupted and a new external base address is registered. Chip selects (S0 and $\overline{\text{S1}}$) are only sampled when a new base address is loaded.

Therefore, the chip selects are registered when either transfer start input is asserted low at the rising edge of the clock (K), and remain latched internally until the next assertion of either $\overline{\text{TSP}}$ or $\overline{\text{TSC}}$. The M62940A Truth Tables and timing diagrams reference specific device operations.

It should be noted that the M62940A allows a non-burst mode of operation where $\overline{\text{TSP}}$ is the $\overline{\text{TS}}$ pin of the MC68040 processor in a typical 2 clock cycle mode of operation, and $\overline{\text{TSC}}$ is held high during C2 (see Figure 7). However, the non-burst mode obviously negates the advantage of the internal burst counter for fast cache fill operations. In either mode (burst or non-burst), the write cycles are internally self-timed, and are initiated by the rising edge of the clock input when $\overline{\text{W}}$ is low.

The $\overline{\text{BAA}}$ input controls subsequent burst data accesses after the first data of the burst cycle is processed. Each time $\overline{\text{BAA}}$ is asserted low for subsequent bursts at the rising edge of the clock

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.
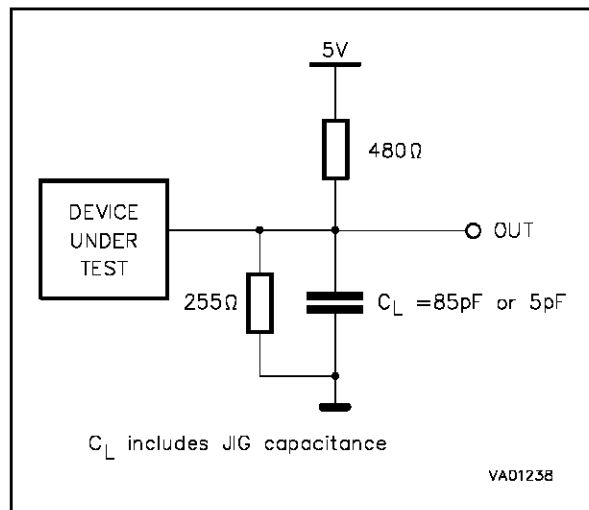
Figure 5. AC Testing Load Circuit

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Table 5. Capacitance[1] ($T_A = 25\ ^\circ C$, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	$V_{IN} = 0V$		5	pF
C_{OUT} [2]	Output Capacitance	$V_{OUT} = 0V$		10	pF

Notes: 1. Sampled only, not 100% tested
2. Outputs deselected

Table 6. DC Characteristics (T_A = 0 to 70 $^\circ$C, V_{CC} = 5V $\pm$ 5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		± 1	μA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		± 1	μA
I_{CC1} [1]	Supply Current	$\overline{G} = V_{IH}$, S0 = V_{IH}, $\overline{S1} = V_{IL}$, All inputs = V_{IL} = 0V and $V_{IH} \geq 3V$		180	mA
I_{CC2} [2]	Supply Current (Standby) TTL	S0 = V_{IL}, $\overline{S1}$ = V_{IH}		40	mA
I_{CC3} [3]	Supply Current (Standby) CMOS	S0 $\leq$ 0.2V, $\overline{S1}$ $\geq$ V_{CC} −0.2V		30	mA
V_{IL}	Input Low Voltage		−0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{KHKH} minimum
2. All other Inputs at $V_{IL} \leq 0.8V$ or $V_{IH} \geq 2.2V$
3. All other Inputs at $V_{IL} \leq 0.2V$ or $V_{IH} \geq V_{CC} - 0.2V$

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Figure 6. General 128K Byte Cache Block Diagram
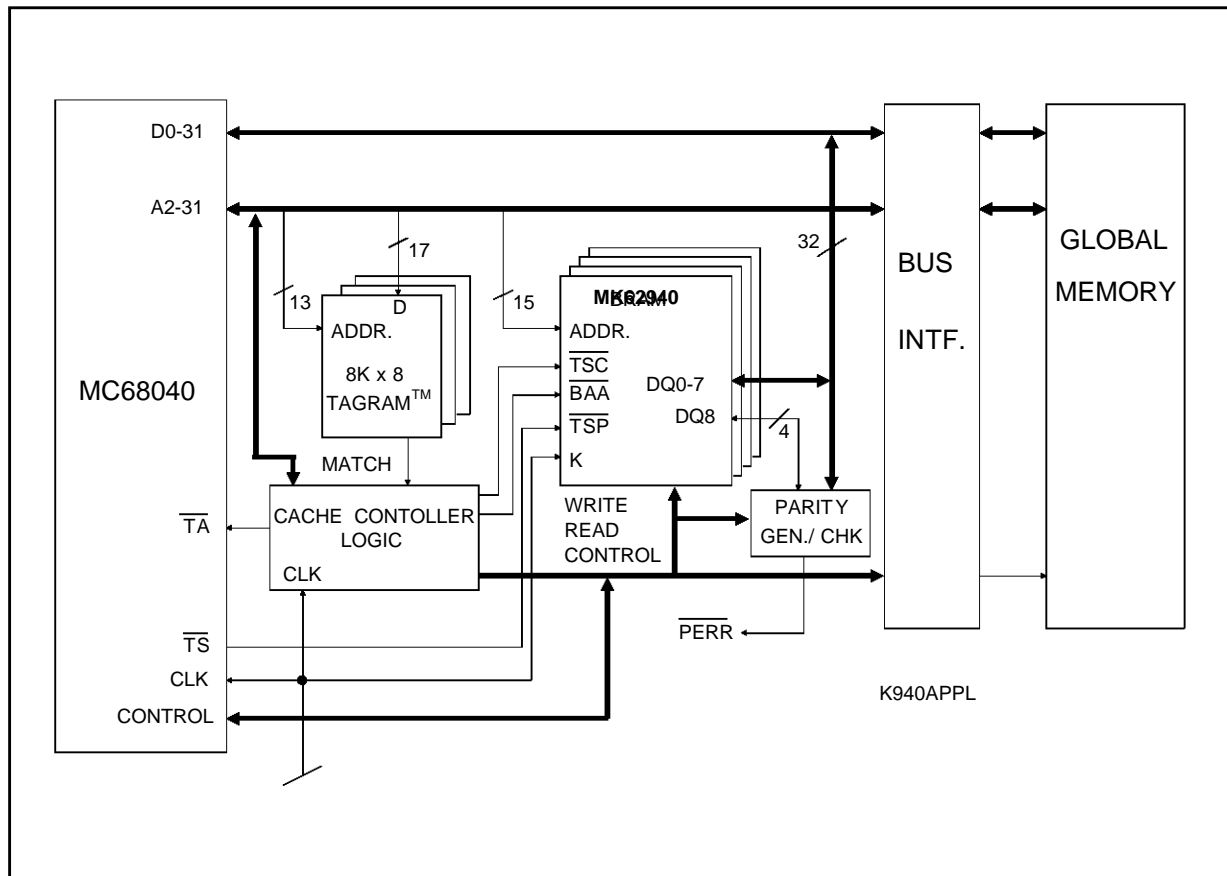
DEVICE OPERATIONS (cont'd)

input, the burst counter is advanced to the next burst address sequence. The address is advanced from the rising edge of K. Wait states can be inserted during burst cycles by holding the $\overline{BAA}$ pin high during positive clock transitions. Upon completion of the full internal burst count, the address will wrap-around to its initial base address.

GENERAL APPLICATION

The M62940A is organized as 32K x 9 bit words to support byte parity. By incorporating TAGRAM™ with a 15 bit tag field and a 15 bit index address, a cache address scheme of 30 bits is monitiored. The TAGRAM in addtion to the M62940A provides an architecture for building a 32K x 32 bit burstable data cache SRAM array, with byte parity, by using four devices in a 128K byte cache application.

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Table 7. Read and Write Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 5%)

Symbol	Parameter	M62940A						Unit	Note
		11		12		14			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{KHKH}	Cycle Time	15		15		20		ns	
t_{KHQV}	Clock Access Time		11		12		14	ns	1
t_{KHKL}	Clock High Pulse Width	5.5		5.5		8		ns	
t_{KLKH}	Clock Low Pulse Width	5.5		5.5		8		ns	
t_{GLQV}	Output Enable Access Time		5		5		6	ns	1
t_{KHQX2}	Clock High to Output Hold Time	3		3		4		ns	2
t_{KHQX1}	Clock High to Output Active	4		4		4		ns	2
t_{GLQX}	Output Enable to Output Active	0		0		0		ns	2
t_{KHQZ}	Clock High to Q High-Z		6		6		6	ns	2
t_{GHQZ}	Output Disable to Q High-Z		6		6		6	ns	2
t_{AVKH}	Address Set-up Time	2		2		3		ns	3
t_{TSVKH}	Transfer Start Set-up Time	2		2		3		ns	3
t_{DVKH}	Data In Set-up Time	2		2		3		ns	3
t_{SWVKH}	Write/Read Set-up Time	2		2		3		ns	3
t_{BAVKH}	Burst Address Advance Set-up Time	2		2		3		ns	3
t_{S0VKH}	Chip Select 0 (S0) Set-up Time	2		2		3		ns	3
t_{S1VKH}	Chip Select 1 ($\overline{S1}$) Set-up Time	2		2		3		ns	3
t_{KHAX}	Address Hold Time	2		2		2		ns	3
t_{KHTSX}	Transfer Start Hold Time	2		2		2		ns	3
t_{KHDX}	Data In Hold Time	2		2		2		ns	3
t_{KHWX}	Write/Read Hold Time	2		2		2		ns	3
t_{KHBAX}	Burst Address Advance Hold Time	2		2		2		ns	3
t_{KHWX}	Asynchronous Write ($\overline{AW}$) Hold Time	2		2		2		ns	3
t_{KHS0X}	Chip Select 0 (S0) Hold Time	2		2		2		ns	3
t_{KHS1X}	Chip Select 1 ($\overline{S1}$) Hold Time	2		2		2		ns	3

Notes: 1. C_L = 85pF (see Figure 5).
2. Transition is measured ± 500 mV from steady-stage voltage with C_L = 5pF (see Figure 5). This parameter is sampled and not 100 % tested.
3. This is synchronous device requiring that all inputs must meet the specified set-up and hold times with stable logic levels for all rising edges of the clock input (K).

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Figure 7. Typical Non-Burst Read/Write Cycles

Note : Typical Non-Burst Bus Cycle   K940R02

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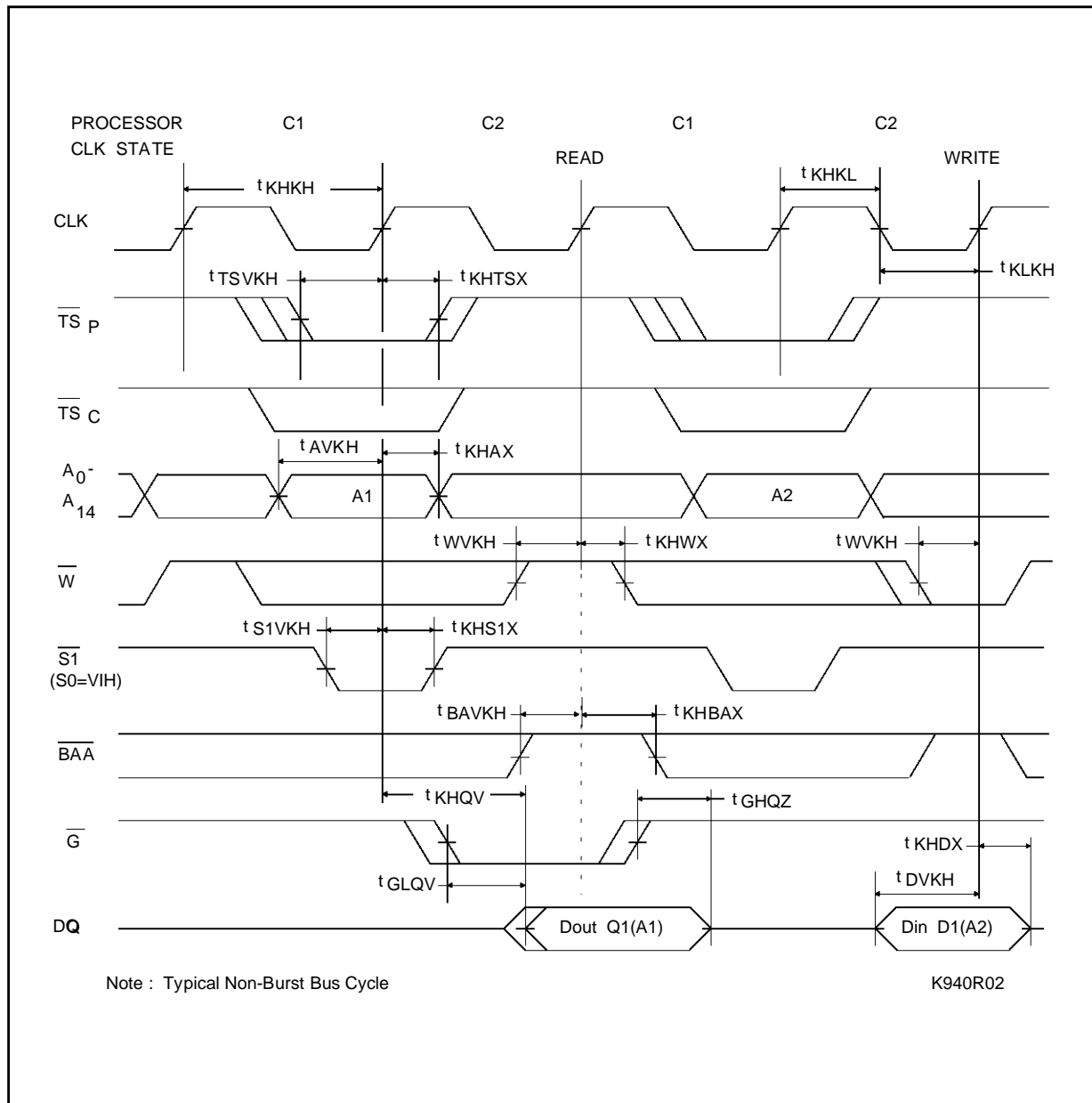
Figure 8. Burst Read Cycle

BRAMBR29

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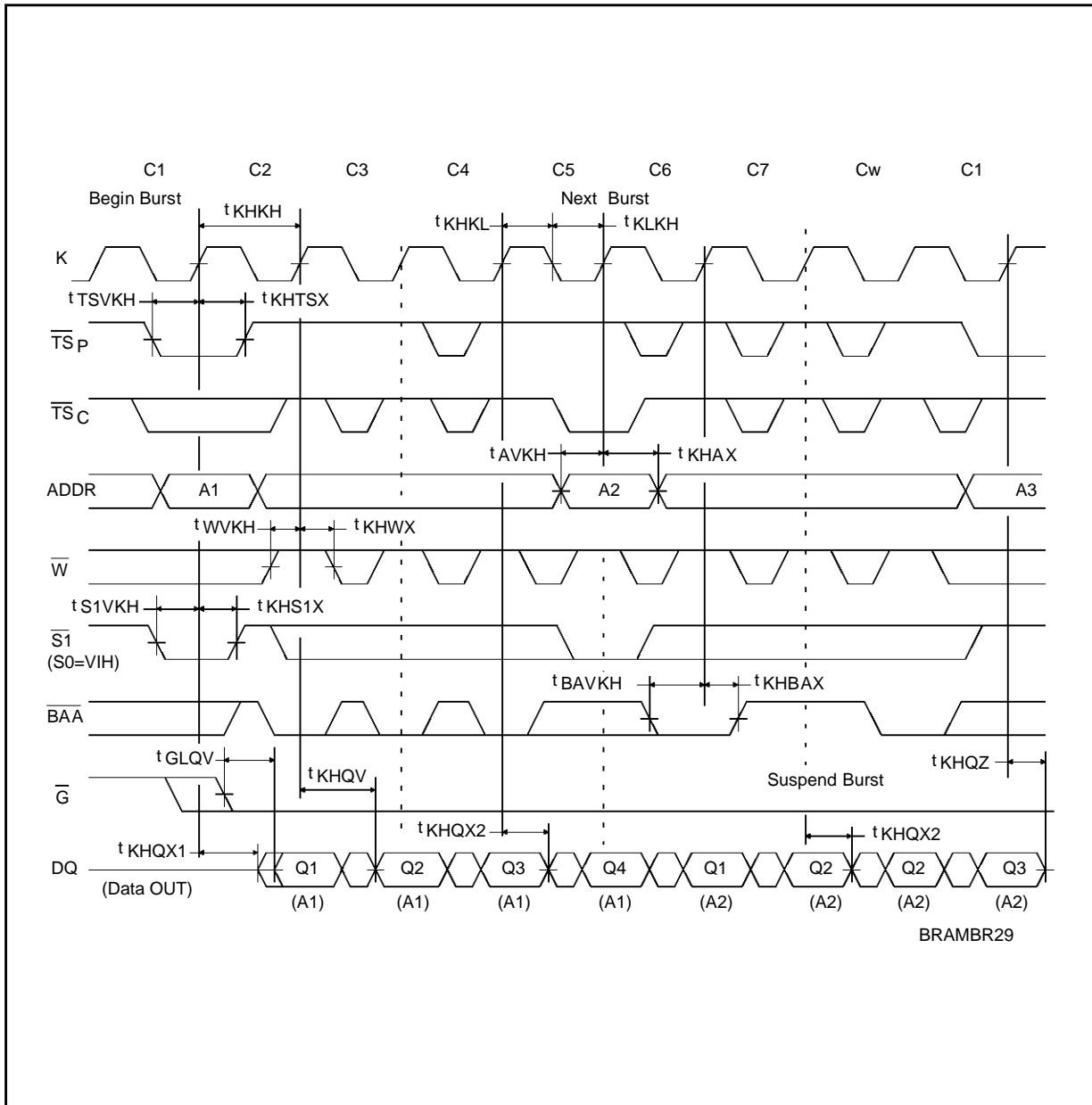
Figure 9. Burst Write Cycle

K940BW02
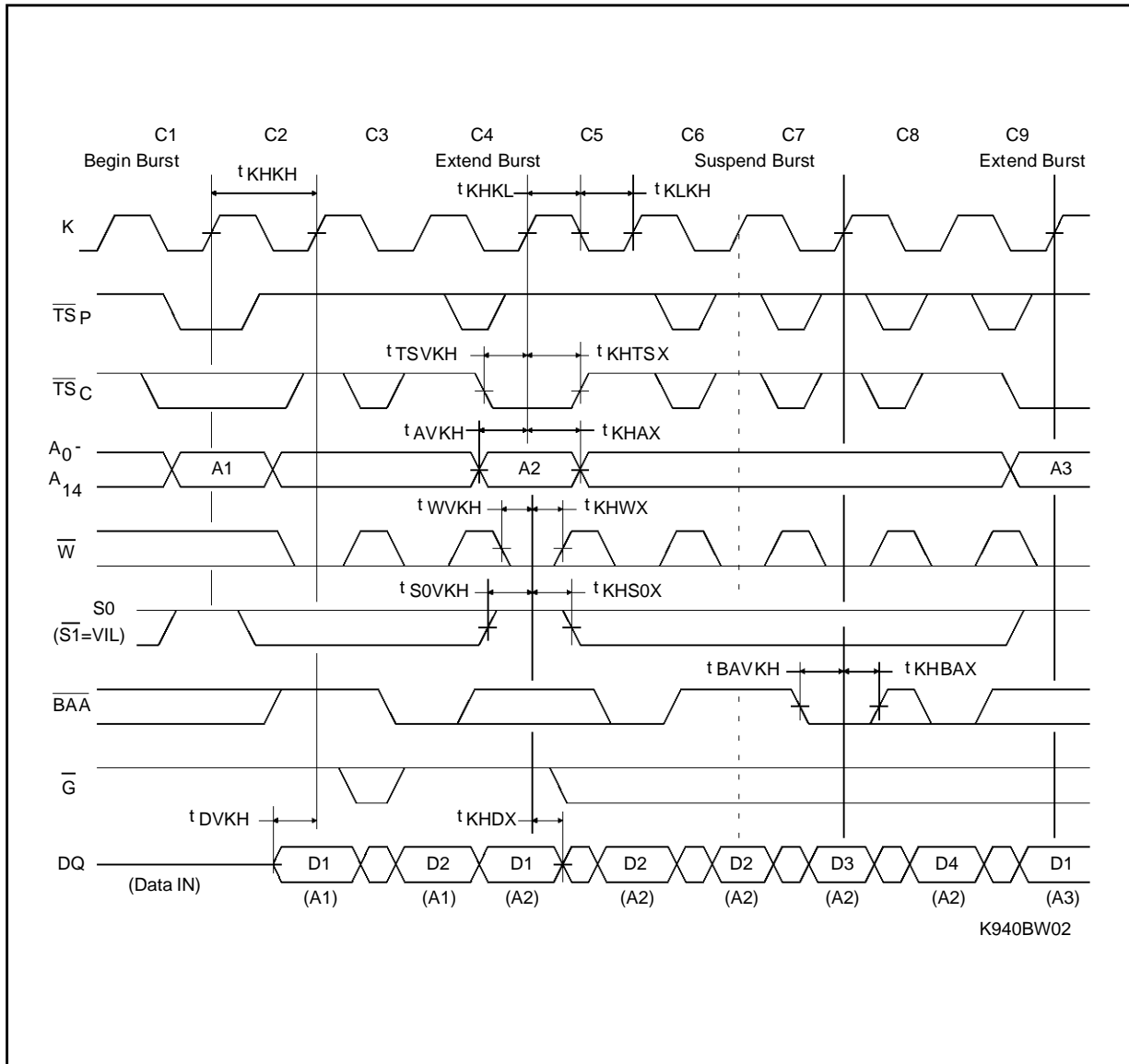
Figure 10. Combined Burst Read/Write Cycle
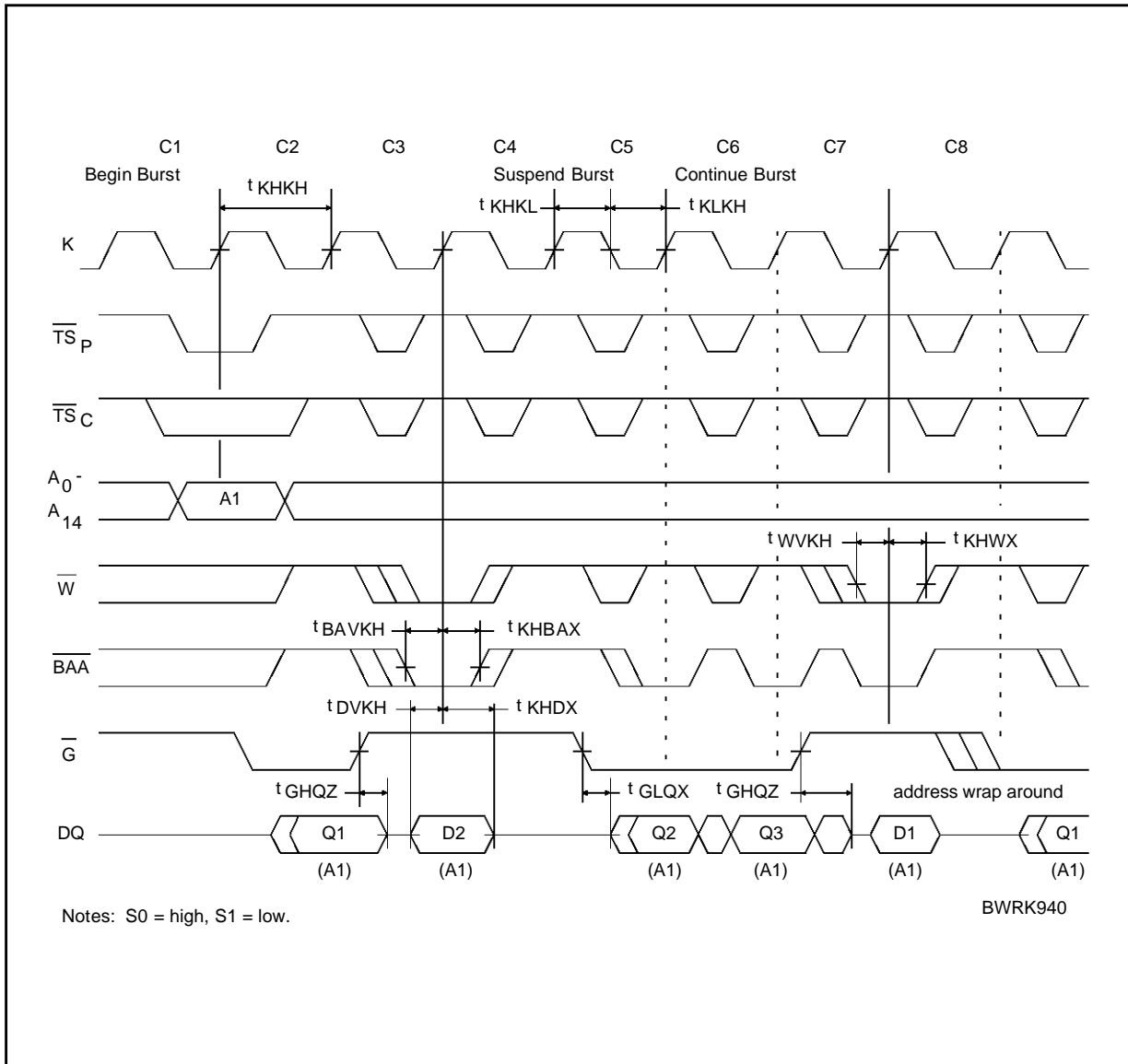
Note: SO = High, $\overline{S1}$ = Low.

ORDERING INFORMATION SCHEME

Example: M62940A   Q 12 TR

Package		Speed		Option	
Q	PLCC44	11	11ns at 66MHz	TR	Tape & Reel Packing
		12	12ns at 66MHz		
		14	14ns at 50MHz		
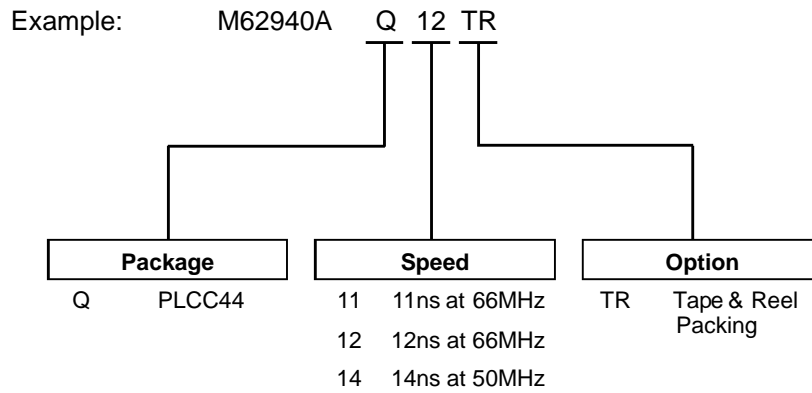
For a list of available options (Package, Speed, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

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PLCC44 - 44 lead Plastic Leaded Chip Carrier, square

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		4.20	4.70		0.165	0.185
A1		2.29	3.04		0.090	0.120
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		17.40	17.65		0.685	0.695
D1		16.51	16.66		0.650	0.656
D2		14.99	16.00		0.590	0.630
E		17.40	17.65		0.685	0.695
E1		16.51	16.66		0.650	0.656
E2		14.99	16.00		0.590	0.630
e	1.27	–	–	0.050	–	–
N		44			44	
CP			0.10			0.004

PLCC44

PLCC

Drawing is out of scale

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